EtherCAT SubDevice Controller Overview (1/3)

as of Feb 2024

Name	AX58100	AX58200	AX58400	TMC8462	ET1100	ET1810/ET1811/ET1812	ET1851/ET1816/ET1817	Anybus NP40	XMC4300	XMC4800
Type	ASIC	ARM MPU	Dual-Core ARM MPU	ASIC	ASIC	Intel (Altera) FPGA + IP Core	Xilinx FPGA + IP Core	ARM MPU	ARM MPU	ARM MPU
Supplier	ASIX	ASIX	ASIX	ADI Trinamic	BECKHOFF	BECKHOFF	BECKHOFF	HMS	Infineon	Infineon
Package	80-pin LQFP 0.4 mm pitch	144-pin HSFBGA 0.8 mm pitch	225LD EHS-TFBGA 0.8 mm pitch	BGA121 0.75 mm pitch	BGA128 0.8 mm pitch	FPGA dependent	FPGA dependent	BGA VF400 0.8 mm pitch	100 LQFP (0.5 mm)	100 LQFP (0.5 mm)
Size	12 x 12 mm	10 x 10 mm	13 x 13 mm	9x9 mm	10 x 10 mm	FPGA dependent	FPGA dependent	17 x 17 mm	16 x 16 mm	20 x 20 mm 16 x 16 mm 12 x 12 mm
µC Interface	SPI/parallel (8/16-bit, asynchronous)	uC bus (Internal, AHB)	uC bus (Internal, AHB)	serial or standalone	serial/parallel (8/16bit, sync/async)*	serial/parallel (8- /16-bit, async) AVALON®*	serial/parallel (8- /16-bit, async) OPB®* and PLB®*	Anybus interface (8- / 16-bit 30 ns parallel, 20 MHz SPI, Shift register, UART)	µC bus (internal, AHB)	µC bus (internal, AHB)
Digital I/O	32	-	20	0..16*	8-32*	8-32*	8-32*	256 / 256 (Shift register mode)	-	-
General Purpose I/O	32	up to 76*	up to 97*	0..24*	0-32*	0-128*	0-128*	-	0 - 46	0 - 123
DPRAM	9 kByte	160 kByte	1 Mbyte	16 kByte	8 kByte	0...60 kByte*	0...60 kByte*	12 kByte	8 kByte	8 kByte
SyncManager Entities	8	8	8	8	8	0...8*	0...8*	4	8	8
FMMU Entities	8	8	8	8	8	0...8*	0...8*	4	8	8
Distributed Clock Support	yes (64-bit)	yes (64-bit)	yes (64-bit)	yes	yes	yes*	yes*	yes	yes (64 Bit)	yes (64 Bit)
No. of Ports	2 (100BaseTX) + Opt. 1 (MII)	2 (100BaseTX) + Opt. 1 (MII)	2 (100BaseTX) + Opt. 1 (MII)	2 (100BaseTX)	2-4 (MII/E-BUS)*	1-3 (MII/max. 2 RMII)	1-3 (MII/max. 2 RMII)	2 (MII)	2 (MII)	2 (MII)
Specials	100BASE-FX support 2 integrated PHYs 3-ch PWM and S/D I/F ABZ and Hall encoder I/F SPI master I/F	2 integrated Ethernet PHYs, USB 2.0 HS OTG, 10/100Mbps Ethernet MAC with RMII and hardware cryptography accelerator 6xLPUARTs, 3xISO-7816-3, 1xQuad-SPI, 3xI2C, 1xI2S, 2xUSCI, 2xCAN, 1xSPI Flash I/F, 2xSDHC, 1x16-ch/12-bit ADC, 2x12-bit DAC, 2xAnalog Comparators, 2xOperational Amplifiers , 4x32-bit timers, 24x16-bit PWM counters, 2xQEI, 1xECAP, supports Real-Time Clock (RTC) , Built-in Die Temperature Sensor (DTS)	Dual-Core 480MHz ARM Cortex-M7 & 240MHz Cortex-M4 MCU, 2 Mbytes embedded Flash memory, 2 ESC Integrated PHY, USB HS OTG, Additional RMII/MII Ethernet MAC with IEEE 1588 for multiprotocol support, TFT-LCD display controller, Security and Cryptographic Accelerator , 96-bit UID, Watchdog, RTC /SysTick timers, Rich communication/control interfaces such as SPI/UART/I2C /I2S/SAI/CAN/SDMMC/ADC/DAC/HDMI-CEC/PWM/DFSDM, etc.	Wide supply range (up to 35V), 2x Integrated DC/DC regulators, 8x Direct High Voltage I/Os, Multi-function I/O block, Integrated PHYs, BGA routable with standard PCB	BGA routable with standard PCB	Various license models and OpenCore Plus are available. A wide range of Intel (former: Altera) FPGAs are supported	Various license models and evaluation Version are available. A wide range of Xilinx FPGAs are supported	Multi-protocol support, ESC Frame forwarding delay: 114 ns, MDP, possible to implement several device profiles	EtherCAT® node on an ARM® Cortex®-M4 processor with up to 256kB on-chip flash, 128kB on-chip RAM and analog/mixed signal capabilities. Qualified for up to 125°C ambient temperature.	EtherCAT® node on an ARM® Cortex®-M4 processor with up to 2MB on-chip flash, 352kB on-chip RAM and analog/mixed signal capabilities. Qualified for up to 125°C ambient temperature.
Further information					https://www.beckhoff.com/ET1100				www.infineon.com/ethercat	www.infineon.com/ethercat
Data Sheet					https://www.beckhoff.com/en-en/products/i-o/ethercat-development-products/				www.infineon.com/ethercat	www.infineon.com/ethercat

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EtherCAT SubDevice Controller Overview (2/3)

as of Feb 2024

Name	netX 500	netX 51	netX 52	netX 90	netX 100	LAN9252	EC-1	RZ/T1	RZ/N2L	RZ/T2M	R-IN32M3-EC	RX72M
Type	ASIC	ASIC	ASIC	ASIC	ASIC	ASIC	ARM MPU	ARM MPU	ARM MPU	ARM MPU	ARM MPU	ARM MPU
Supplier	hilscher	hilscher	hilscher	hilscher	hilscher	Microchip	Renesas	Renesas	Renesas	Renesas	Renesas	Renesas
Package	BGA345 1 mm pitch	PBGA324 1 mm pitch	PBGA244 1 mm pitch	LFBGA144 0.8 mm pitch	BGA345 1 mm pitch	64 pin QFN (0.5 mm pitch) 64 pin TQFP-EP (0.5 mm pitch)	196 pin BGA (0.8 mm)	FBGA320 0.8 mm pitch	FBGA225, 0.8mm pitch FBGA121, 0.8mm pitch	FBGA320, 0.8mm pitch FBGA225, 0.8mm pitch	BGA324 1 mm pitch	LFBGA224, 0.8mm pitch LFBGA176, 0.8mm pitch LFQFP176, 0.5mm pitch LFQFP144, 0.5mm pitch LFQFP100, 0.5mm pitch
Size	22 x 22 mm	19 x 19 mm	15 x 15 mm	10 x 10 mm	22 x 22 mm	9 x 9 mm 12 x 12 mm	12 x 12 mm	17 x 17 mm	13 x 13 mm 10 x 10 mm	17 x 17 mm 13 x 13 mm	19 x 19 mm	LFBGA224: 13 x 13 mm LFBGA176: 13 x 13 mm LFQFP176: 24 x 24 mm LFQFP144: 20 x 20 mm LFQFP100: 14 x 14 mm
µC Interface	µC bus (internal, 32bit)	µC bus (internal, 32bit)	µC bus (internal, 32bit)	µC bus (internal, 32bit)	µC bus (internal, 32bit)	Host Bus/SPI/SQI	USB Host/Function, CAN, SCIFA, I2C RSPI, Flash	16/32-bit parallel and various serial (SPI/I2C/UART)	USB Host/Function, CAN-FD, SPI, SCI, DSMIF, I2C, xSPI, External BUS IF(SRAM/SDRAM/Host IF)	USB Host/Function, CAN-FD, SPI, SCI, DSMIF, I2C, xSPI, External BUS IF(SRAM/SDRAM)	16/32-bit parallel (master/slave) and serial (SPI/I2C/UART)	USB, CAN, UART, SPI, I2C, SCI, QSPI
Digital I/O	-	-	-	-	-	0-16*	-	-	-	-	-	44
General Purpose I/O	16	32	24	16	16	0-16*	115* GPIOs / 8 Input (port multiplexed, partial 5V-tolerant, open drain, input pull-up)	0-209*	0-134*	0-193*	0-96*	0-182*
DPRAM	256/512 Byte (Mailbox/Process Data)	6 kByte	6 kByte	6 kByte	256/512 Byte (Mailbox/Process Data)	4 kByte	512 KB (ATCM) with ECC 32 KB (BTCM) with ECC	8 kByte	8 kByte	8 kByte	8 kByte	8 kByte
SyncManager Entities	4	8	8	8	4	4	8	8	8	8	8	8
FMMU Entities	3	8	8	8	3	3	8	8	8	8	8	8
Distributed Clock Support	yes	yes	yes	yes	yes	yes	yes (64 bit)	yes	yes	yes	yes	yes (64 bit)
No. of Ports	2 (100BaseTX)	2 (100BaseTX)	2 (100BaseTX)	2 (100BaseTX)	2 (100BaseTX)	2 (100BaseTX) + opt. 1 (MII)	2 (MII)	2 (RMII/MII)	3 (RGMII/RMII/MII)	3 (RGMII/RMII/MII)	2 (100BaseTX)	2 (100BaseTX/MII/RMII)
Specials	Multi-protocol support, Integrated PHYs, Integrated µC (ARM9-200MHz)	Multi-protocol support, Integrated PHYs, Integrated µC (ARM9-100MHz)	Multi-protocol support, Integrated PHYs, Integrated µC (ARM9-100MHz)	Multi-protocol support, Integrated PHYs, Integrated µC, OnChip Flash 1,5 Mbytes, OnChip DC-DC Converter, (ARM Cortex M4-100MHz) Additional integrated Application Controller (ARM Cortex M4 - 100 MHz)	Multi-protocol support, Integrated PHYs, Integrated µC (ARM9-200MHz)	Cable Diagnostics, 100FX support, 2 integrated PHYs, integrated 1.2V regulator	Safety Functions, Multi-Function Pin Controller	Additional Ethernet port (RMII/MII), 2-axis high-speed motion control support, digital encoder interfaces (EnDat, BiSS, others), Multi-protocol support, security option, functional safety support, Cortex-R4F (450/600MHz), Cortex-M3 (150MHz) cores	Multi-protocol support (EtherCAT, etc), Optimized for network companion chip (parallel bus slave, xSPI slave interface to connect external application CPU), One chip solution for various applications, Functional safety support, Cortex-R52 (400MHz) core	Multi-protocol support (EtherCAT, etc), Optimized for motor control (2-axis high-speed motion control support, digital encoder interfaces (EnDat, BiSS, others, etc.), Functional safety support, Cortex-R52 Dual (800MHz) cores	Multi-protocol support, SPI, I2C, UART, 1.3 Mbyte int. RAM, <1W typical incl. 2 PHYs	Multi-protocol support (EtherCAT, etc.), Security option, Encryption option, 105 °C operating temperature support, Functional safety support
Further information	https://www.hilscher.com/netx	https://www.hilscher.com/netx	https://www.hilscher.com/netx	https://www.hilscher.com/netx	https://www.hilscher.com/netx	www.microchip.com/wwwproducts/en/LAN9252	www.renesas.com/en-eu/ec-1	www.renesas.eu/products/mpumcu/rz/index.jsp	www.renesas.com/rzn2l	www.renesas.com/rzt2m	www.renesas.eu/automation	———
Data Sheet						www.microchip.com/wwwproducts/en/LAN9252		www.renesas.eu/products/mpumcu/rz/Documentation.jsp	https://www.renesas.com/us/en/document/dst/rzn2l-group-datasheet	https://www.renesas.com/us/en/document/dst/rzt2m-group-datasheet	www.renesas.eu/r-in	

*configurable

EtherCAT SubDevice Controller Overview (3/3)

as of Feb 2024

EtherCAT Technology Group

Name	ANTAIOS	TRITON	C2000™ (TMS320F28388D/S)	Sitara AMIC110 SoC	Sitara AM3357/9	Sitara AM4377/9	Sitara AM571xE	Sitara AM572xE	Sitara AM65x SoC	Sitara AM64x SoC	Sitara AM243x SoC	Sitara AM263x SoC
Type	ARM MPU	ARM MPU	TI C28x subsystem(s) with ARM Connectivity Manager	ARM MPU	ARM MPU	ARM MPU	ARM MPU	ARM MPU	ARM MPU	ARM MPU	ARM MCU	ARM MCU
Supplier	YASKAWA	YASKAWA	Texas Instruments	Texas Instruments	Texas Instruments	Texas Instruments	Texas Instruments	Texas Instruments	Texas Instruments	Texas Instruments	Texas Instruments	Texas Instruments
Package	TFBGA-380 (0.65 mm pitch) TFBGA-385 (0.8 mm pitch)	FCBGA-784 (0.8 mm pitch)	337 BGA 0.8mm pitch 176 QFP 0.5mm pitch	324-pin NFBGA 0.8mm pitch	324-pin NFBGA 0.8 mm pitch	491-pin NFBGA, 0.65mm pitch (0.8 mm effective routing)	760-pin FCBGA 0.8 mm pitch	760-pin FCBGA 0.8 mm pitch	784-pin S-PBGA 0.8mm pitch	441-pin FCBGA 0.8mm pitch	441-pin FCBGA 0.8mm pitch / 293-pin FCCSP 0.5mm pitch via channel array	324-pin NFBGA 0.8mm pitch
Size	15 mm x 15 mm 19 mm x 19 mm	23 mm x 23 mm	16 x16 mm 26 x 26 mm	15x15mm	15 x 15 mm	17 x 17 mm	23 x 23 mm	23 x 23 mm	23mmx23mm	17.2mmx17.2mm	17.2mmx17.2mm / 11mmx11mm	15mmx15mm
µC Interface	SPI / QSPI / 16 Bit asynchronous interface	SPI / QSPI / 16 Bit asynchronous interface	16-bit async PDI interface	200MHz interconnect (internal, 32bit)	200 MHz interconnect (internal, 32bit)	200 MHz interconnect (internal, 32bit)	200 MHz interconnect (internal, 32bit)	200 MHz interconnect (internal, 32bit)	250MHz interconnect (internal, 256bit)	250MHz interconnect (internal, 128bit)	250MHz interconnect (internal, 128bit), SPI (external)	200MHz interconnect (internal, 64bit)
Digital I/O	26Bits Input, 20Bits Output	32Bits Input, 22Bits Output	N/A	8	8	8	8	8	8	8	8	8
General Purpose I/O	up to 32	up to 32	32	>32	> 32	> 32	> 32	> 32	>32	>32	>32	>32
DPRAM	up to 64 kByte	up to 64 kByte	16 kByte	8 kByte	8 kByte	28 kByte	28 kByte	28 kByte	60 kByte	60 kByte	60 kByte	28 kByte
SyncManager Entities	8	8	8	8	8	8	8	8	8	8	8	8
FMMU Entities	8	8	8	8	8	8	8	8	8	8	8	8
Distributed Clock Support	yes (64 bit)	yes (64 bit)	yes	yes	yes	yes	yes	yes	yes	yes	yes	yes
No. of Ports	2 (100BaseTX) or 2 (MII)	4 Gbit Ethernet port	2 (MII)	2 (MII)	2 (MII)	2 (MII)	2 (MII)	2 (MII)	2 (MII)	2 (MII)	2 (MII)	2 (MII)
Specials	Multi fieldbus protocol support, 2 x integrated PHYs, 1 x integrated GBit Ethernet MAC, Integrated ARM® Cortex®-A5 (288MHz), Backplane communication: SliceBus master for profichip's SNAP+ ASIC, Integrated technology module (2xSII / 4xPWM / 4xCounter), QuadSPI interface (e.g. NOR Flash for firmware), DDR2 external memory interface, Other external interfaces: SD/MMC, NAND, USB2 device, SRAM master/slave, SPI master/slave	Multi fieldbus protocol support, 2 port Real-Time Ethernet switch with integrated PHYs, 2x integrated GBit Ethernet MAC,3 Integrated ARM® Cortex®-A17 (1.26GHz), Secure Core, Backplane communication: SliceBus master for profichip's SNAP+ ASIC, Integrated technology module (2xSII / 4xPWM / 4xCounter), QuadSPI interface (e.g. NOR Flash for firmware), DDR4 external memory interface, 3 PCI Express® Controller, Other external interfaces: 3 SD/MMC, NAND, USB2 device, SRAM master/slave, SPI master/slave	EtherCAT slave enabled real-time controller. Up to 925 MIPS. Single or dual C28x + CLA control subsystems for real-time control loops. Arm based Connectivity Manager for communictions and host control. On-chip flash, RAM, 4x 16-bit ADC, SDFM, 32-ch PWM, analog comparator subsystem, multiple communications ports, configurable logic block for CPLD/FPGA replacement and absolue encoder support.	Entire EtherCAT slave controller can be implemented on internal memory (no external DDR needed), Industrial Communications Subsystem (PRU-ICSS) for multi-protocol support, CAN	Industrial Communications Subsystem (PRU-ICSS) for multi-protocol support, Gigabit Switch, CAN, display, ARM Cortex-A8 (275MHz-1000MHz)	Multi-protocol support, Second PRU-ICSS for Motor control (EnDat, sigma delta filtering etc), Gigabit Switch, CAN, Display subsystem, 2D/3D graphics, Camera I/F, Optional secure boot, ARM Cortex-A9 (upto 1 GHz)	Dual Industrial Communications Subsystem (PRU-ICSS) for multi-protocol support (2 EtherCAT slave instances or EtherCAT slave to protocol gateway), Motor control (EnDat, sigma delta filtering), 2D/3D Graphics, Display subsystem, Video acceleration, PCIe, SATA, Optional secure boot, ARM Cortex-A15 (upto 1.5 GHz), 2x M4 cores, 2x C66x DSP core	Dual Industrial Communications Subsystem (PRU-ICSS) for multi-protocol support (2 EtherCAT slave instances or EtherCAT slave to protocol gateway), 2D/3D Graphics, Display subsystem, Video acceleration, PCIe, SATA, Optional secure boot, 2x ARM Cortex-A15 (upto 1.5 GHz), 2x M4 cores, 2x C66x DSP cores	Entire ESC can be implemented on internal memory (no external DDR needed), 3x Gigabit Industrial Communications Subsystem (PRU_ICSSG) for multi protocol support (up to 3 EtherCAT slave instances), PRU_ICSSG also supports Motor Control functionality (Encoder feedback such as Hiperface-DSL and EnDat and Sigma Delta filtering), up to 4x Arm Cortex-A53 cores at 1.1GHz, 2x Cortex-R5F core at 400MHz with optional lock-step for functional safety or other purposes, 2MB on-chip SRAM	Entire ESC can be implemented on internal memory (no external DDR needed), Dual Gigabit Industrial Communications Subsystem (PRU_ICSSG) for multi protocol support (2 EtherCAT slave instances or EtherCAT slave to protocol gateway), PRU_ICSSG also supports Motor Control functionality (Encoder feedback such as Hiperface-DSL and EnDat and Sigma Delta filtering), up to 4x Arm Cortex-R5F cores at 800MHz, up to 2x Cortex-A53 cores at 1GHz, 1x Cortex-M4 core at 400MHz for functional safety or other purposes, 2MB on-chip SRAM	Entire ESC can be implemented on internal memory (no external DDR needed), Dual Gigabit Industrial Communications Subsystem (PRU_ICSSG) for multi protocol support (2 EtherCAT slave instances or EtherCAT slave to protocol gateway), PRU_ICSSG also supports Motor Control functionality (Encoder feedback such as Hiperface-DSL and EnDat and Sigma Delta filtering), up to 4x Arm Cortex-R5F cores at 800MHz, 1x Cortex-M4 core at 400MHz for functional safety or other purposes, 2MB on-chip SRAM	Entire EtherCAT slave controller can be implemented on internal memory, Industrial Communications Subsystem (PRU_ICSS), PRU_ICSS also supports Motor Control functionality (Encoder feedback such as Hiperface-DSL and EnDat and Sigma Delta filtering), up to 4x Arm Cortex-R5F cores at 400MHz, 2MB on-chip SRAM
Further information			www.ti.com/product/tms320f28388d	www.ti.com/amic110	www.ti.com/AM335x	www.ti.com/AM437x	www.ti.com/product/AM5718	www.ti.com/product/AM5728	www.ti.com/product/am6548	www.ti.com/product/am6442	www.ti.com/product/am2434	www.ti.com/product/am2634
Data Sheet			www.ti.com/lit/gpn/tms320f28388d	http://www.ti.com/product/AMIC110/datasheet	www.ti.com/lit/ds/symlink/am3359.pdf	www.ti.com/lit/ds/symlink/am4379.pdf	www.ti.com/lit/ds/symlink/am5718.pdf	www.ti.com/lit/ds/symlink/am5728.pdf	http://www.ti.com/product/am6548/datasheet	http://www.ti.com/product/am6442/datasheet	http://www.ti.com/product/am2434/datasheet	http://www.ti.com/product/am2634/datasheet

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